What is claimed is:

1. A semiconductor device provided with a plurality of memory transistors comprising:

an active layer comprising a source region, a drain region and a channel forming region;

a first insulating film formed on the active layer;

a floating gate formed on the first insulating film;

a second insulating film formed on the floating gate; and

a control gate formed on the second insulating film,

a first region and a second region included in the channel forming region,

means for intercepting charge injection from the first region to the floating gate;

means for carrying out charge injection from the second region to the floating gate; and

means for stopping charge injection from the second region to the floating gate.

2. A semiconductor device according to claim 1, wherein a thickness of the first insulating film formed on the first region is thicker than a thickness of the first insulating film formed on the second region.

3. A semiconductor device according to claim 1, wherein a concentration of impurity elements added to the first and second regions is respectively different.

4. A semiconductor device according to claim 1, wherein the memory transistor stores multi-value information.

5. A semiconductor device according to claim 1, wherein the memory transistor is formed on a substrate selected from the group consisting of a single crystal semiconductor substrate, a substrate having an insulating surface and a SOI substrate.

6. A semiconductor device according to claim 1, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

7. A semiconductor device provided with a plurality of memory transistors

comprising:

an active layer comprising a source region, a drain region and a channel forming region;

a first insulating film formed on the active layer;

a floating gate formed on the first insulating film;

a second insulating film formed on the floating gate; and

a control gate formed on the second insulating film,

a first region and a second region included in the channel forming region,

means for intercepting charge drawing from the floating gate to the first region;

means for carrying out charge drawing from the floating gate to the second region;

means for stopping charge drawing from the floating gate to the second region.

8. A semiconductor device according to claim 7, wherein a thickness of the first insulating film formed on the first region is thicker than a thickness of the first insulating film formed on the second region.

9. A semiconductor device according to claim 7, wherein a concentration of impurity elements added to the first and the second regions is respectively different.

10. A semiconductor device according to claim 7, wherein the memory transistor stores multi-value information.

11. A semiconductor device according to claim 7, wherein the memory transistor is formed on a substrate selected from the group consisting of a single crystal semiconductor substrate, a substrate having an insulating surface and a SOI substrate.

12. A semiconductor device according to claim 7, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

13. A semiconductor device provided with a plurality of memory cells in which first and second memory transistors are connected in series, comprising:

an active layer comprising a source region, a drain region, a first channel

forming region of the first memory transistor and a second channel forming region of the second memory transistor;

a first insulating film formed on the active layer;

a first floating gate of the first memory transistor and a second floating gate of the second memory transistor formed on the first insulating film;

a second insulating film formed on the first and the second floating gates; and

a first control gate of the first memory transistor and a second control gate of the second memory transistor formed on the second insulating film,

means for intercepting charge injection from the first channel forming region to the first floating gate;

means for carrying out charge injection from the second channel forming region to the second floating gate; and

means for stopping charge injection from the second channel forming region to the second floating gate,

wherein the first and second floating gates are connected to each other, and

wherein the first and second control gates are connected to each other.

14. A semiconductor device according to claim 13, wherein a thickness of the first insulating film on the first channel forming region is thicker than a thickness of the first insulating film on the second channel forming region.

15. A semiconductor device according to claim 13, wherein a concentration of impurity elements in the first channel forming region is different from a concentration of impurity elements in the second channel forming region.

16. A semiconductor device according to claim 13, wherein the second memory transistor stores multi-value information.

17. The semiconductor device according to claim 13, wherein the first and the second memory transistors are formed on a substrate selected from the group consisting of a single crystal semiconductor substrate, a substrate having an insulating surface and a SOI substrate.

18. A semiconductor device according to claim 13, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback

apparatus, a personal computer and a portable information terminal.

19. A semiconductor device according to claim 13, wherein a threshold voltage of the first channel forming region is different from a threshold voltage of the second channel forming region.

20. A semiconductor device according to claim 13, wherein the semiconductor device further comprises a means for self-concluding charge injection from the second channel forming region to the second floating gate when an amount of an electric charge reaches an amount of an electric charge predetermined by a difference between a threshold of the first memory transistor and a threshold of the second memory transistor and by voltage provided with the memory cell.

21. A semiconductor device provided with a plurality of memory cells in which first and second memory transistors are connected in series, comprising:

an active layer comprising a source region, a drain region, a first channel forming region of the first memory transistor and a second channel forming region of the second memory transistor;

a first insulating film formed on the active layer;

a first floating gate of the first memory transistor and a second floating gate of the second memory transistor formed on the first insulating film;

a second insulating film formed on the first and second floating gates; and

a first control gate of the first memory transistor and a second control gate of the second memory transistor formed on the second insulating film,

means for intercepting charge drawing from the first floating gate to the first channel forming region;

means for carrying out charge drawing from the second floating gate to the second channel forming region; and

means for stopping charge drawing from the second floating gate to the second channel forming region,

wherein the first and second floating gates are connected to each other, and

wherein the first and second control gates are connected to each other.

22. A semiconductor device according to claim 21, wherein a thickness of the first insulating film on the first channel forming region is thicker than a thickness of the first insulating film on the second channel forming region.

23. A semiconductor device according to claim 21, wherein a concentration of impurity elements in the first channel forming region is different from a concentration of impurity elements in the second channel forming region.

24. A semiconductor device according to claim 21, wherein the second memory transistor stores multi-value information.

25. A semiconductor device according to claim 21, wherein the first and the second memory transistors are formed on a substrate selected from the group consisting of a single crystal semiconductor substrate, a substrate having an insulating surface and a SOI substrate.

26. A semiconductor device according to claim 21, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

27. A semiconductor device according to claim 21, wherein a threshold voltage of the first channel forming region is different from a threshold voltage of threshold channel forming region.

28. A semiconductor device according to claim 27, wherein the semiconductor device further comprises a means for self-concluding charge drawing from the second floating gate to the second channel forming region when amount of an electric charge reaches amount of an electric charge predetermined by a difference between a threshold of the first memory transistor and a threshold of the second memory transistor and voltage provided with the memory cell.

29. A semiconductor device comprising:

an active layer having a drain region, a source region, and a channel forming region formed over a substrate;

a first region and a second region formed in the channel forming region;

a first insulating film formed on the active layer;

a floating gate formed on the first insulating film;

a second insulating film formed on the floating gate; and

a control gate formed on the second insulating film,

wherein a concentration of impurity elements in the first region is lager than a

concentration of impurity elements in the second region;

wherein a thickness of the first insulating film on the second region is thinner than a thickness of the second insulating film on the first region.

30. A semiconductor device according to claim 29, wherein a threshold of the first region is lager than a threshold of the second region.

31. A semiconductor device according to claim 29, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

32. A semiconductor device comprising:

an active layer comprising a first channel forming region interposed between a source region and a source/drain region and a second channel forming region interposed between the source/drain region and a drain region formed over a substrate;

a first insulating film formed on the active layer;

a first floating gate and a second floating gate formed on the first insulating film;

a second insulating film formed on the first and the second floating gates;

a first control gate and a second control gate formed on the second insulating film;

wherein a concentration of impurity elements in the first channel forming region is lager than a concentration of impurity elements in the second channel forming region; and

wherein a thickness of the first insulating film on the second channel forming region is thinner a thickness of the first insulating film on the first channel forming region.

33. A semiconductor device according to claim 32, wherein a threshold of the first channel forming region is lager than a threshold of the second channel forming region.

34. A semiconductor device according to claim 32, wherein the semiconductor device is an electronic device selected from the group consisting of a video camera, a digital camera, a head-mount type of display, a DVD player, a game

machine, a goggle type of display, a car navigation apparatus, an acoustic playback apparatus, a personal computer and a portable information terminal.

35. A microprocessor comprising a CPU core, a cache memory, a flush memory, a clock controller, a cache controller, and a serial interface, an I/O port, at least one of the cache memory and the flush memory comprising:

an active layer comprising a drain region, a source region, and a channel forming region formed over a substrate;

a first region and a second region formed in the channel forming region;

a first insulating film formed on the active layer;

a floating gate formed on the first insulating film;

a second insulating film formed on the floating gate; and

a control gate formed on the second insulating film,

wherein a concentration of impurity elements in the first region is lager than a concentration of impurity elements in the second region;

wherein a thickness of the first insulating film on the second region is thinner than a thickness of the second insulating film on the first region.

36. A microprocessor according to claim 35, wherein a threshold of the first region is lager than a threshold of the second region.

37. A semiconductor device comprising an involatile memory comprising a memory transistor, a correction circuit, a source signal side drive circuit, a gate signal side drive circuit, a pixel portion, the memory transistor comprising:

an active layer comprising a drain region, a source region, and a channel forming region formed over a substrate;

a first region and a second region formed in the channel forming region;

a first insulating film formed on the active layer;

a floating gate formed on the first insulating film;

a second insulating film formed on the floating gate; and

a control gate formed on the second insulating film.

wherein a concentration of impurity elements in the first region is lager than a concentration of impurity elements in the second region;

wherein a thickness of the first insulating film on the second region is thinner than a thickness of the second insulating film on the first region.

38. A semiconductor device according to claim 37. wherein a threshold of the first region is lager than a threshold of the second region.

39. A microprocessor comprising a CPU core, a cache memory, a flush memory, a clock controller, a cache controller, and a serial interface, an I/O port, at least one of the cache memory and the flush memory comprising:

an active layer comprising a first channel forming region interposed between a source region and a source/drain region and a second channel forming region interposed between the source/drain region and a drain region formed over a substrate:

a first insulating film formed on the active layer;

a first floating gate and a second floating gate formed on the first insulating film;

a second insulating film formed on the first and the second floating gates;

a first control gate and a second control gate formed on the second insulating film;

wherein a concentration of impurity elements in the first channel forming region is lager than a concentration of impurity elements in the second channel forming region; and

wherein a thickness of the first insulating film on the second channel forming region is thinner a thickness of the first insulating film on the first channel forming region.

40. A microprocessor according to claim 39, wherein a threshold of the first channel forming region is lager than a threshold of the second channel forming region.

41. A semiconductor device comprising an involatile memory comprising a memory transistor, a correction circuit, a source signal side drive circuit, a gate signal side drive circuit, a pixel portion, the memory transistor comprising:

an active layer comprising a first channel forming region interposed between a source region and a source/drain region and a second channel forming region interposed between the source/drain region and a drain region formed over a substrate:

a first insulating film formed on the active layer;

a first floating gate and a second floating gate formed on the first insulating film;

a second insulating film formed on the first and the second floating gates:

a first control gate and a second control gate formed on the second insulating film;

wherein a concentration of impurity elements in the first channel forming region is lager than a concentration of impurity elements in the second channel forming region; and

wherein a thickness of the first insulating film on the second channel forming region is thinner a thickness of the first insulating film on the first channel forming region.

42. A semiconductor device according to claim 41, wherein a threshold of the first channel forming region is lager than a threshold of the second channel forming region.